



Preliminary

XRD9824/26EVAL

September 2000-3

XRD9824/26EVAL

Evaluation System

User Manual

EVALUATION KIT PART LIST

This kit contains the following:

- XRD9824/26EVAL Application Board
- XRD9824 or XRD9826 20 pin SOIC
- XRD9824/26EVAL User Manual
- XRD9824 or XRD9826 Datasheet

FEATURES

- CIS or CCD Scanner Analog Front End
- Easy Evaluation of the XRD9824 or XRD9826
- Accessible I/O Interface for Common Laboratory Equipment
- Optimized Layout with Four Layers

INTRODUCTION

The XRD9824/26EVAL is a complete printed circuit board for characterizing EXAR's XRD9824 or XRD9826. The XRD9824/26 are fully integrated, high performance analog signal processors with a 14/16-Bit analog-to-digital converter. The XRD9824/26 is specifically designed for use in CIS or CCD imaging applications. CIS scanners use the S/H, PGA and digital programmable offset. CCD scanners use the CDS, PGA and digital programmable offset.

This application board combines a proven PC board layout with optimized analog and digital interface circuitry to satisfy the requirements needed in evaluating high performance devices of this type. The XRD9824/26EVAL contains the device being tested, latches for the output data and I/O headers for a flexible user interface. Complete AC and DC performance of the parts can be evaluated by interfacing external laboratory equipment.

System Configuration-Lab Setup

The XRD9824/26EVAL application board is set up as a common test circuit. Figure 1. shows a block diagram of the default test Configuration. See Figures 2., 3. and 4. for schematic pages and circuit details.

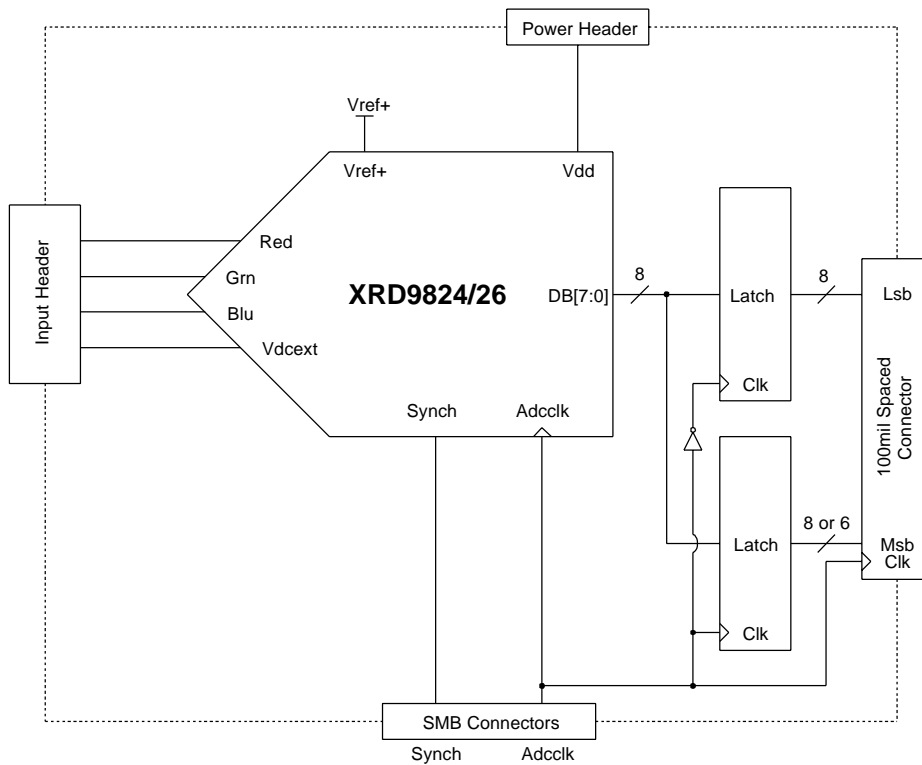
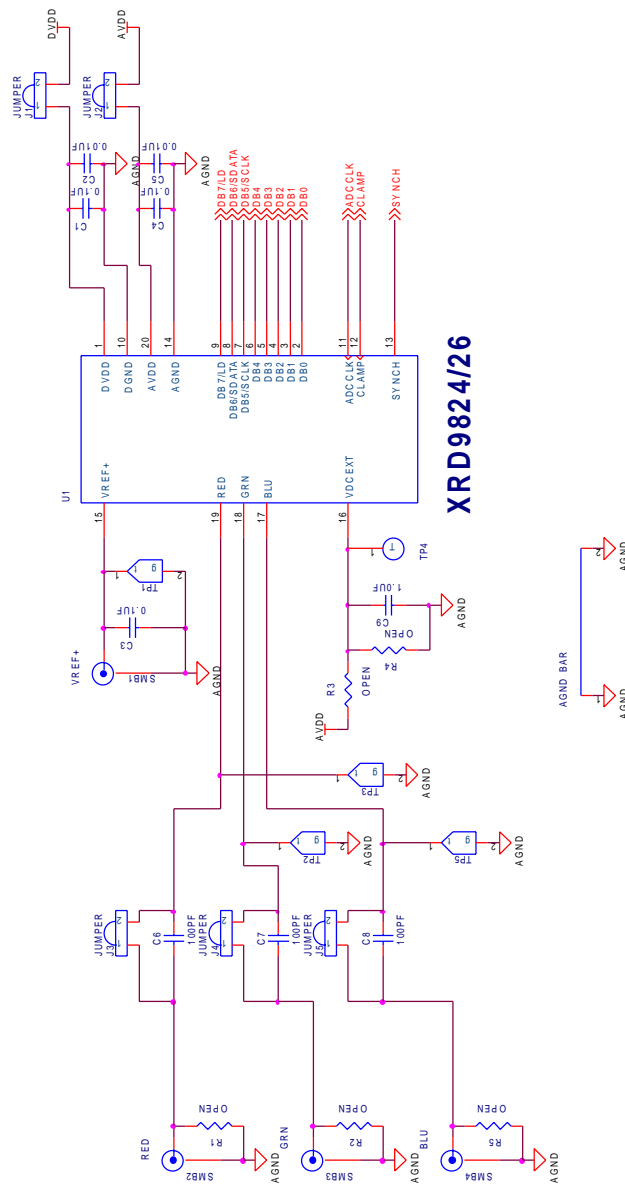


Figure 1. Block Diagram of the XRD9824/26EVAL Application Board

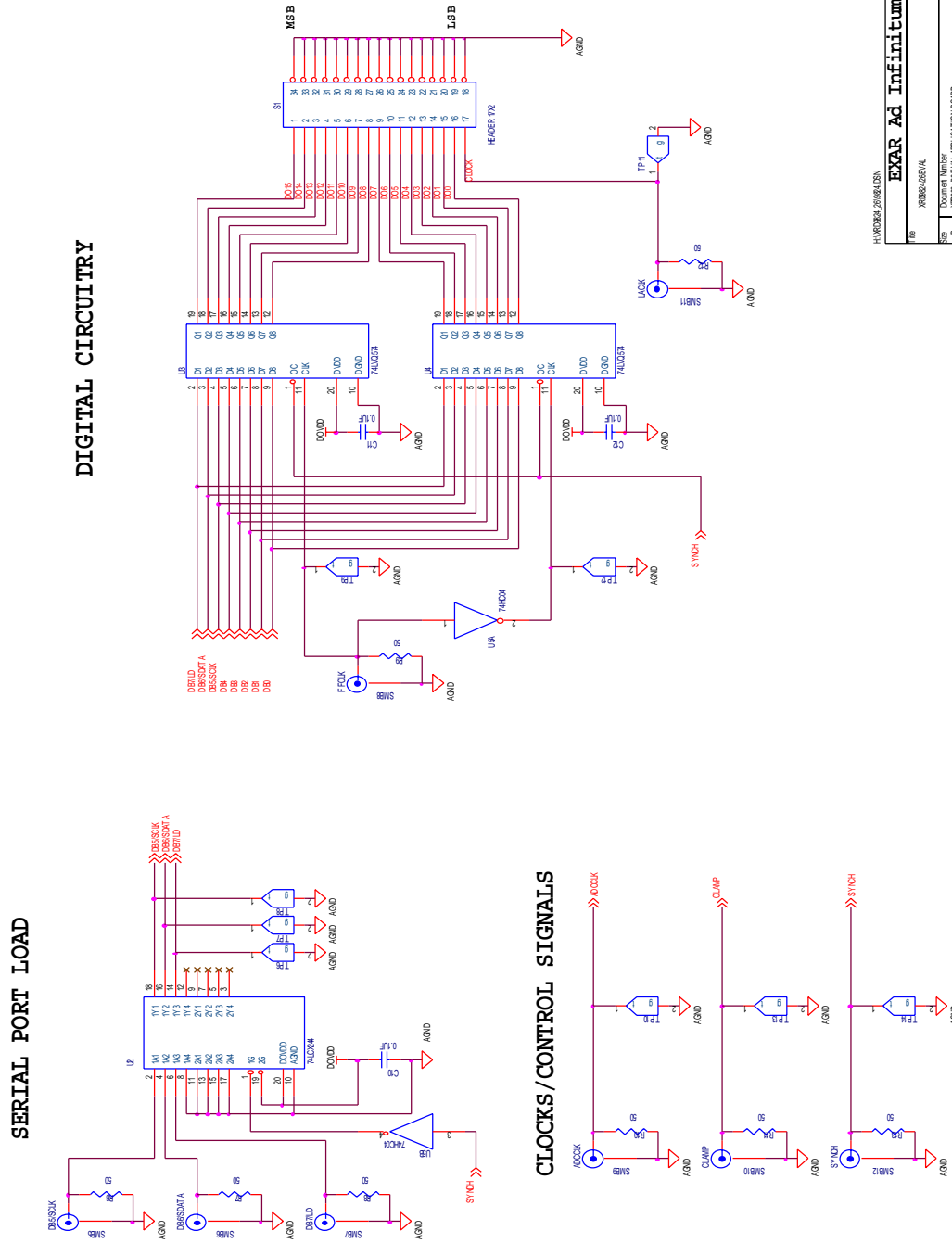
XRD9824/26 ANALOG CIRCUITRY



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Rev	A
Date	Monday, September 11, 2000
Sheet	1 of 3

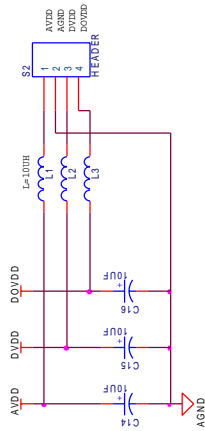
Figure 2. Schematic Page 1 of the XRD9824/26EVAL Application Board



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Figure 3. Schematic Page 2 of the XRD9824/26EVAL Application Board

POWER HEADER



UNUSED CIRCUITRY

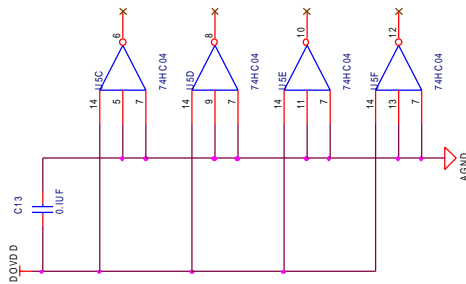


Figure 4. Schematic Page 3 of the XRD9824/26EVAL Application Board

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	FIG: 3 of 3

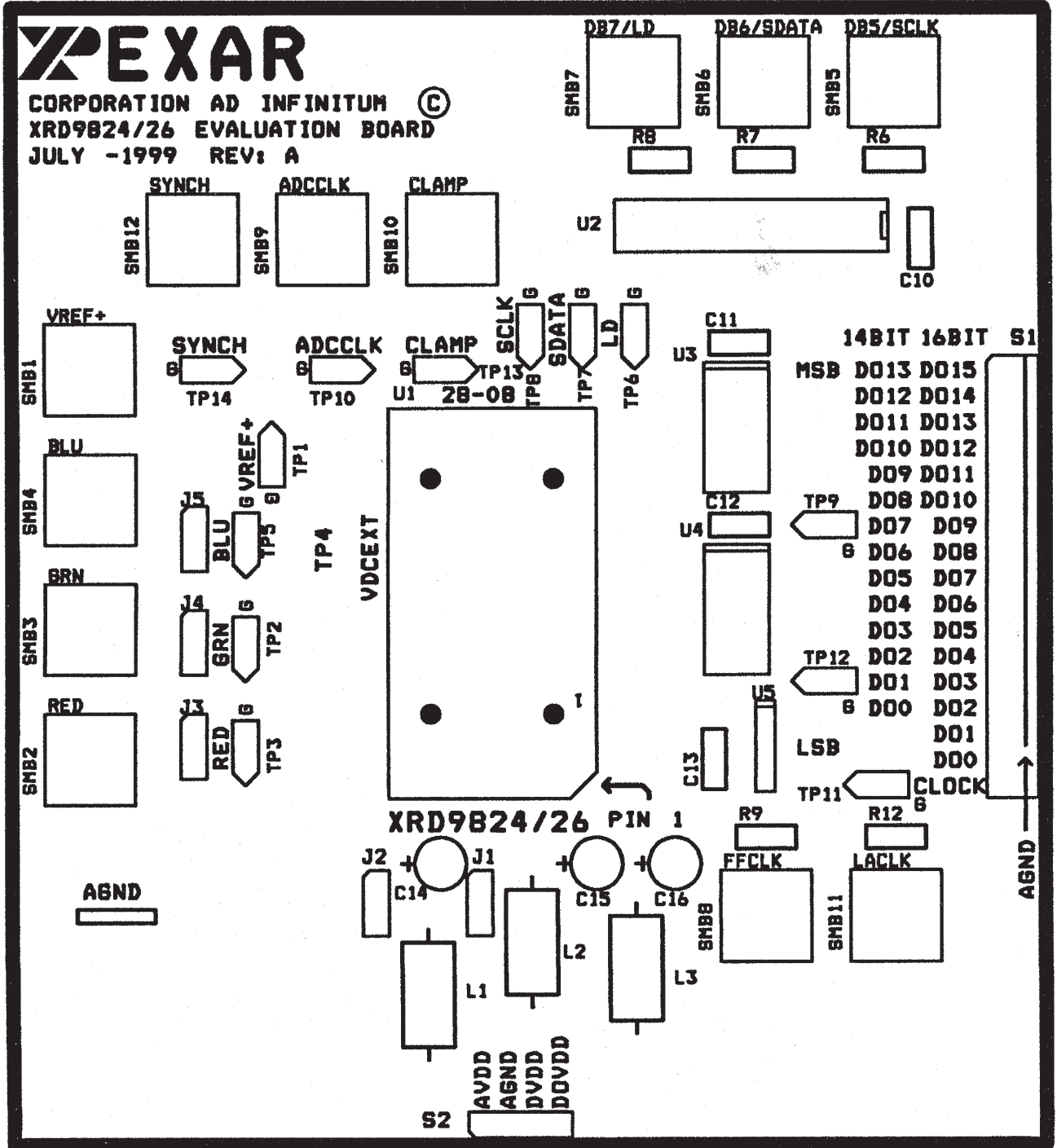


Figure 5. Top Silk Screen

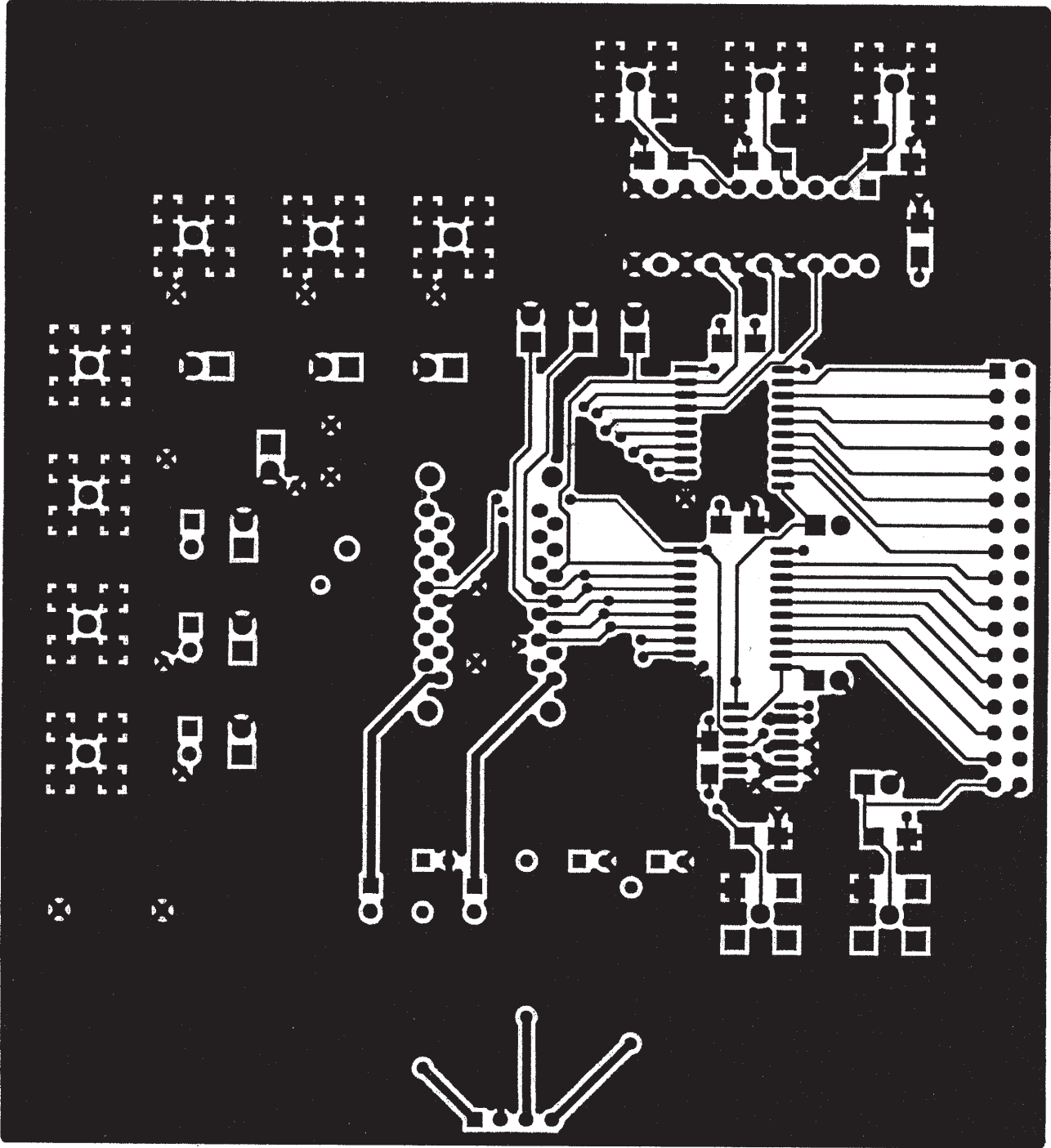


Figure 6. Top Layer

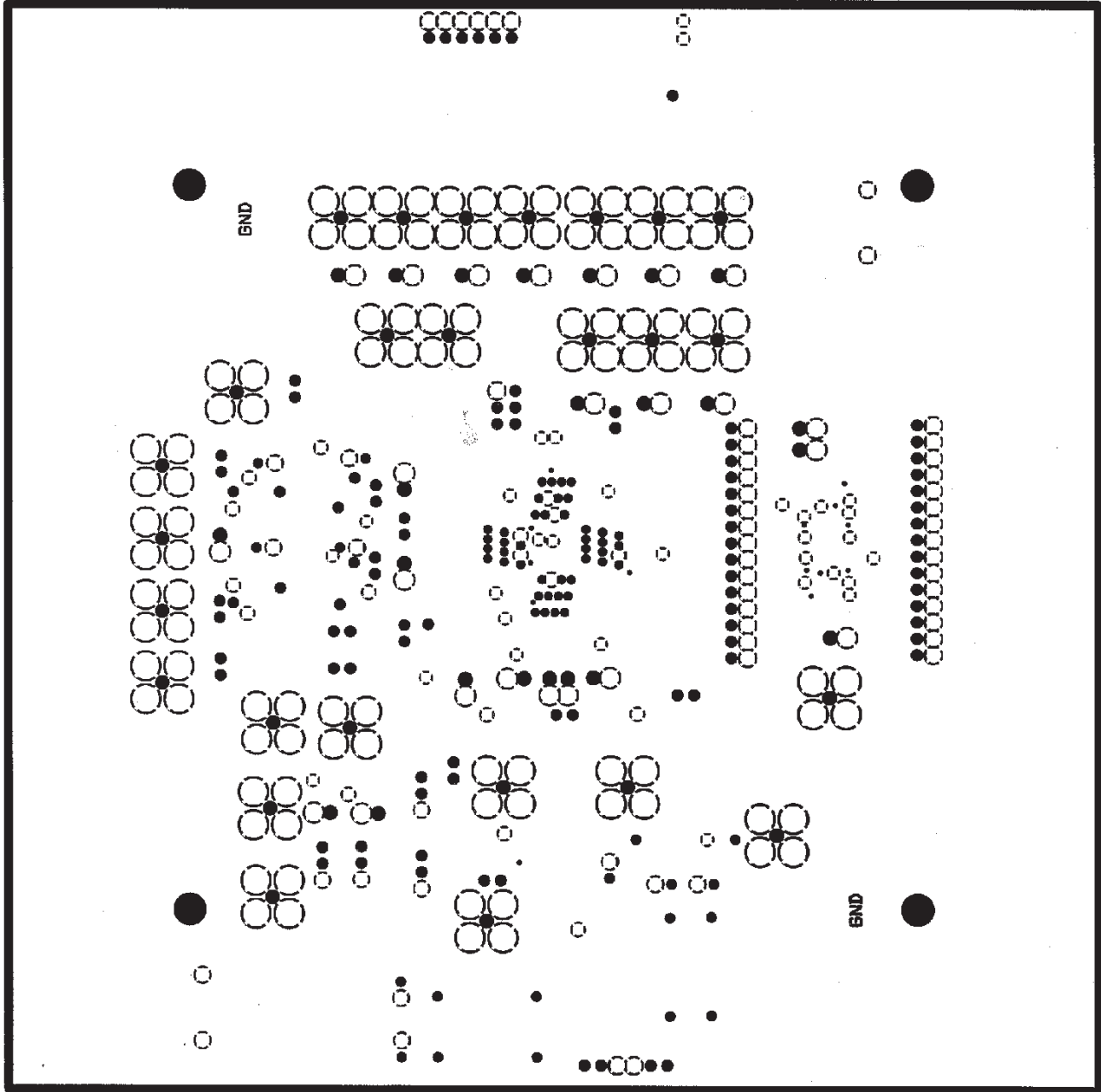


Figure 7. Ground Layer

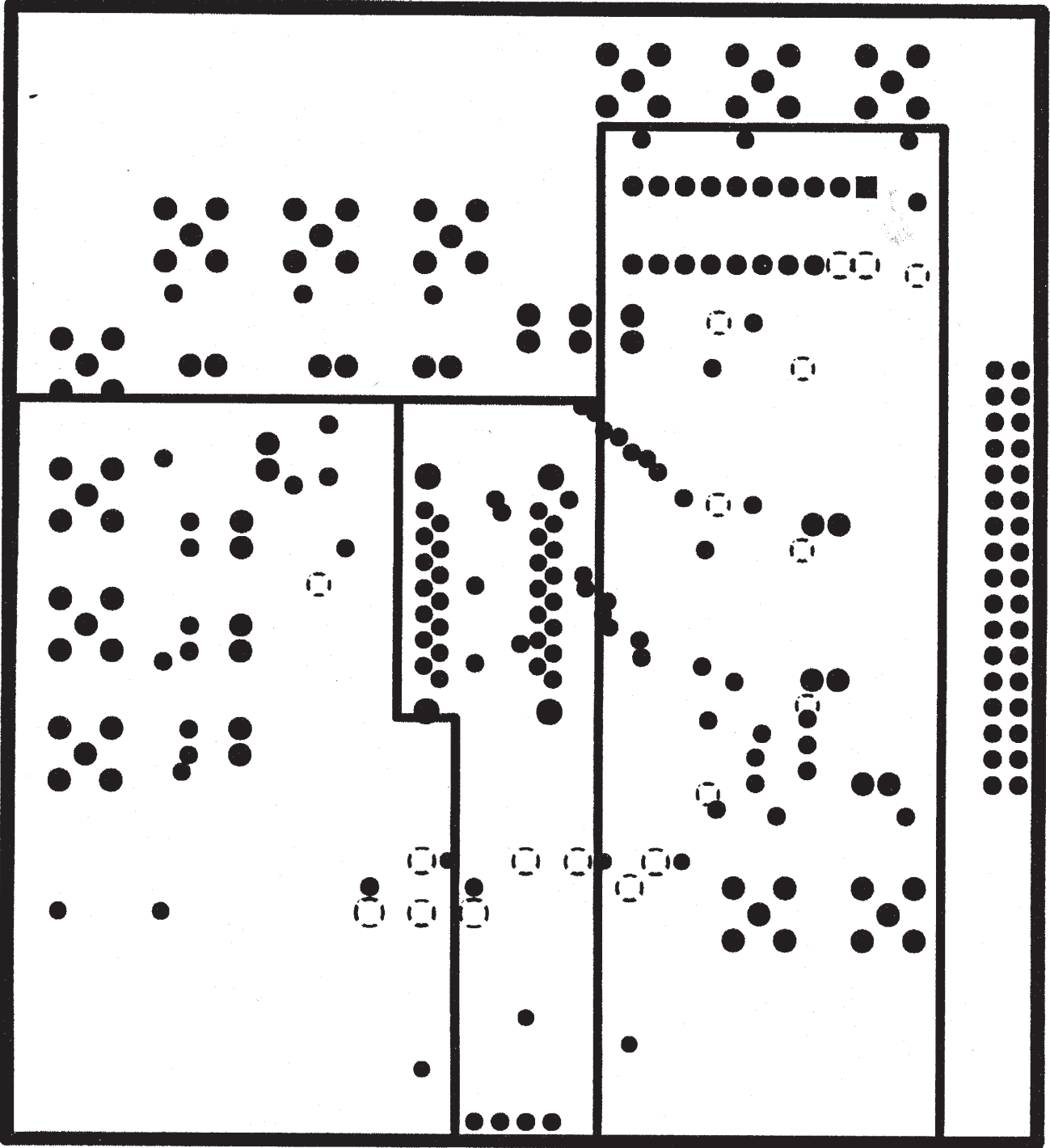


Figure 8. Power Layer

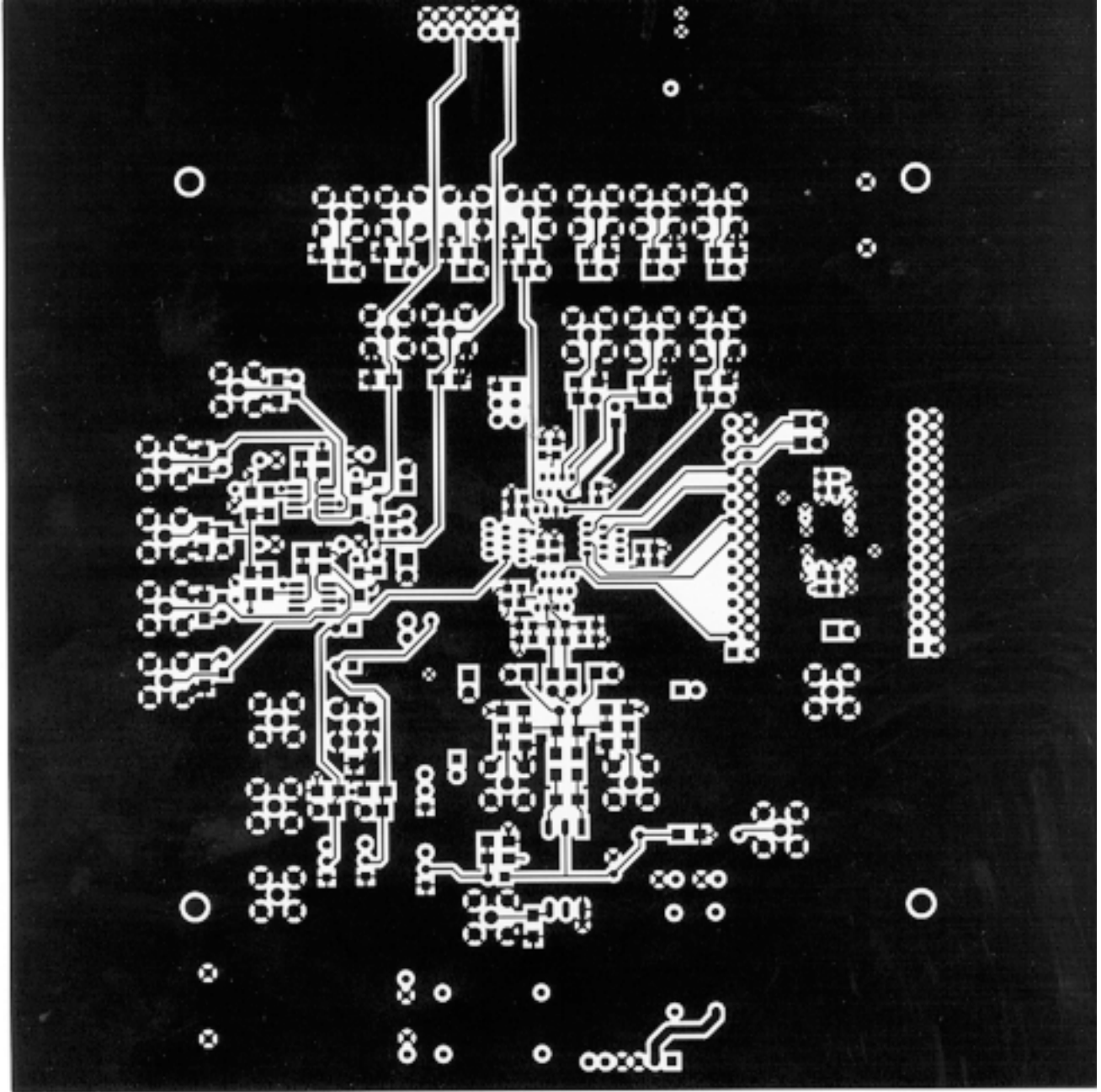


Figure 9. Bottom Layer

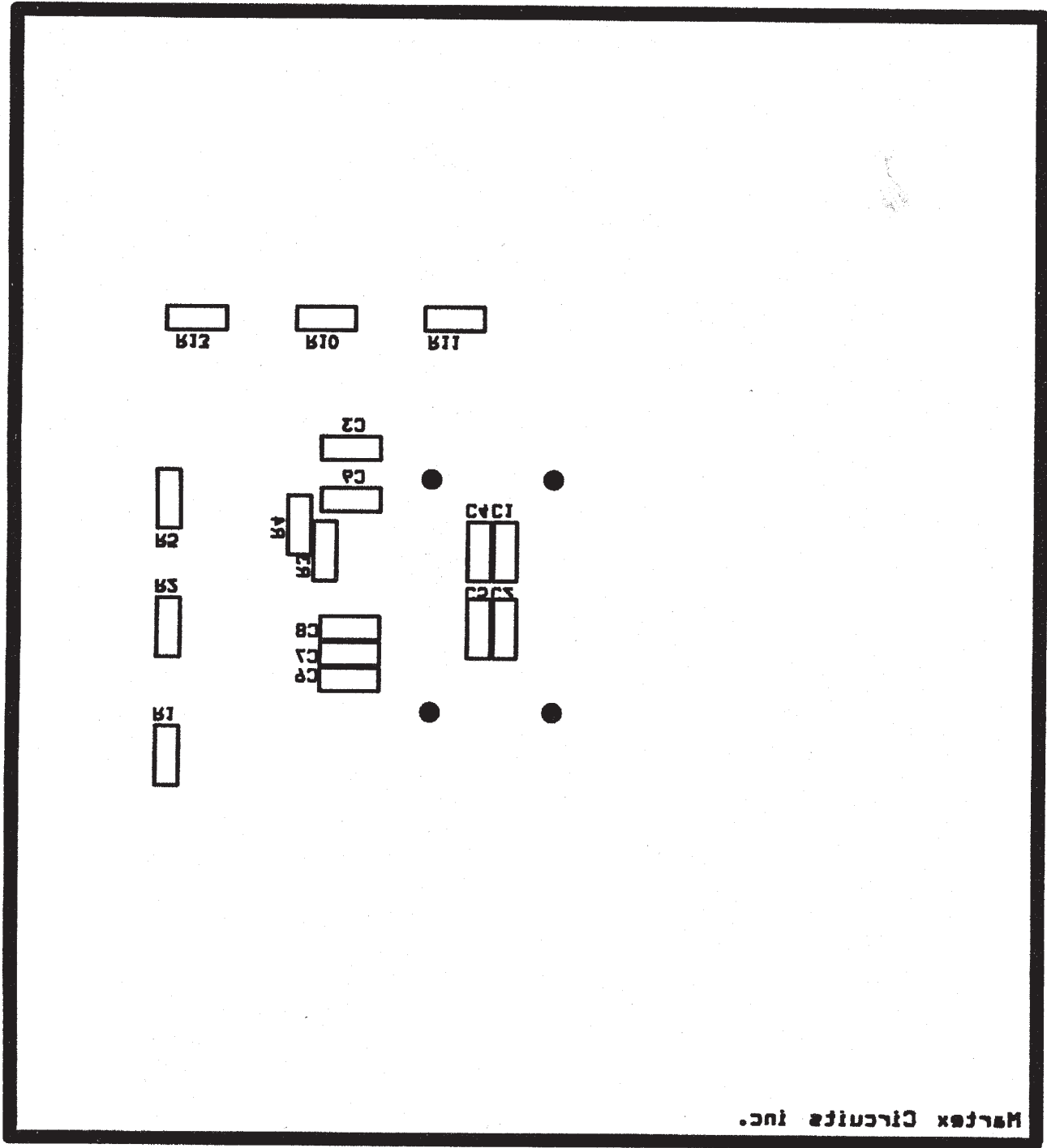


Figure 10. Bottom Silk Screen



Notes

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